WHAT IS CLAIMED IS:

1. A phase locked loop, comprising:

a voltage controlled oscillator operable to generate an output carrier signal having a controlled frequency;

a sigma delta modulator operable to generate a dither control signal; and

a phase interpolator operable to receive one or more phase signals, each of the phase signals being delayed with respect to the output carrier signal, the phase interpolator operable to generate an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal.

2. The phase locked loop of claim 1, wherein the interpolated output signal is a weighted sum of one or more of the one or more phase signals.

3. The phase locked loop of claim 2, further comprising:

a divider to receive the interpolated output signal from the phase interpolator, the divider operable to divide the interpolated output signal based in part on the dither control

signal and generate a divided output signal.

4. The phase lock loop of claim 3, wherein the divider is a fractional N divider operable to fractionally divide the interpolated output signal.

5. The phase lock loop of claim 3, wherein the divider is an integer only divider operable to divide the interpolated output signal by integers.

6. The phase lock loop of claim 3, wherein the voltage controlled oscillator is a multiphase voltage controlled oscillator operable to generate one or more delay signals, each of the one or more delay signals being delayed by a predetermined time period with respect to the output carrier signal.

7. The phase lock loop of claim 6, wherein one or more of the one or more input phases are derived based at least in part from the one or more delay signals.

8. The phase lock loop of claim 3, further comprising a prescaler operable to generate one or more of the one or more

phase signals for the phase interpolator.

9. The phase lock loop of claim 3, further comprising a phase-frequency detector operable to compare a reference signal to the divided output signal and generate an error signal corresponding to a frequency difference between the reference signal and the divided output signal.

10. The phase lock loop of claim 9, further comprising a charge pump operable to convert the error signal into a charge pump output signal.

11. The phase lock loop of claim 10, further comprising a loop filter operable to smooth the charge pump output signal and generate a voltage controlled oscillator control signal to control the voltage controlled oscillator.

12. A method comprising:

generating an output carrier signal having a controlled frequency;

generating a dither control signal;

generating one or more phase signals, each of the phase signals being delayed with respect to the output carrier

signal; and

interpolating the phase signals and generating an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal.

13. The method of claim 12, wherein the interpolated output signal is a weighted sum of one or more of the one or more phase signals.

14. The method of claim 13, further comprising:

dividing the interpolated output signal based in part on the dither control signal and generating a divided output signal.

15. The method of claim 14, wherein the divided output signal is fractionally divided with respect to the interpolated output signal.

16. The method of claim 14, wherein the divided output signal is divided by an integer with respect to the interpolated output signal.

17. The method of claim 14, wherein generating an output carrier signal having a controlled frequency includes generating a delay signal delayed by a predetermined time period with respect to the output carrier signal.

18. The method of claim 17, wherein one or more of the one or more phase signals are generated based at least in part on the one or more delay signals.

19. The method of claim 14, further comprising generating one or more of the one or more phase signals to be interpolated based at least in part on frequency division.

20. The method of claim 14, further comprising:

comparing a reference signal to the divided output signal; and

generating an error signal corresponding to a phase difference between the reference signal and the divided output signal.

21. The method of claim 20, further comprising converting the error signal into a charge pump output signal.

22. The method of claim 21, further comprising, smoothing the charge pump output signal and generating a voltage controlled oscillator control signal to control a voltage controlled oscillator.

23. A phase locked loop, comprising:

means for generating an output carrier signal having a controlled frequency;

means for generating a dither control signal; and

means for receiving one or more phase signals, each of the phase signals being delayed with respect to the output carrier signal, and generating an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal.

24. The phase lock loop of claim 23, wherein the interpolated output signal is a weighted sum of one or more of the one or more phase signals.

25. The phase lock loop of claim 24, further comprising:

means for dividing the interpolated output signal based in part on the dither control signal and generating a divided

output signal.

26. The phase lock loop of claim 25, wherein the means for dividing is operable to fractionally divide the interpolated output signal.

27. The phase lock loop of claim 25, wherein the means for dividing is operable to divide the interpolated output signal by integers.

28. The phase lock loop of claim 25, wherein the means for generating an output carrier signal is operable to generate one or more delay signals, each of the one or more delay signals being delayed by a predetermined time period with respect to the output carrier

29. The phase lock loop of claim 28, wherein one or more of the one or more input phases are derived based at least in part from the one or more delay signals.

30. The phase lock loop of claim 25, further comprising means for generating one or more of the one or more phase signals.

31. The phase lock loop of claim 25, further comprising means for comparing a reference signal to the divided output signal and generating an error signal corresponding to a frequency difference between the reference signal and the divided output signal.

32. The phase lock loop of claim 31, further comprising pumping means for converting the error signal into a charge pump output signal.

33. The phase lock loop of claim 32, further comprising means for smoothing the charge pump output signal and generating a voltage controlled oscillator control signal to control the voltage controlled oscillator.

34. A wireless transceiver, comprising:

a transmitter operable to transmit a modulated carrier signal, the transmitter including a phase lock loop operable to control a frequency of the modulated carrier signal, the phase lock loop including,

a voltage controlled oscillator to generate the modulated carrier signal having a controlled frequency;

a sigma delta modulator operable to generate a

dither control signal; and

a phase interpolator operable to receive a predetermined number of phase signals, each of the phase signals being delayed with respect to the output carrier signal, the phase interpolator operable to generate an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal.

35. The wireless transceiver of claim 34, wherein the interpolated output signal is a weighted sum of one or more of the one or more phase signals.

36. The wireless transceiver of claim 35, wherein the phase locked loop further includes a divider to receive the interpolated output signal from the phase interpolator, the divider operable to divide the interpolated output signal based in part on the dither control signal and generate a divided output signal.

37. The wireless transceiver of claim 36, wherein the divider is a fractional N divider operable to fractionally divide the

interpolated output signal.

38. The wireless transceiver of claim 36, wherein the divider is an integer only divider operable to divide the interpolated output signal by integers.

39. The wireless transceiver of claim 36, wherein the voltage controlled oscillator is a multiphase voltage controlled oscillator operable to generate one or more delay signals, each of the one or more delay signals being delayed by a predetermined time period with respect to the output carrier signal.

40. The wireless transceiver of claim 39, wherein one or more of the one or more input phases are derived based at least in part from the one or more delay signals.

41. The wireless transceiver of claim 36, wherein the phase locked loop further includes a prescaler operable to generate one or more of the one or more phase signals for the phase interpolator.

42. The wireless transceiver of claim 36, wherein the phase locked loop further includes a phase-frequency detector operable to compare a reference signal to the divided output signal and generate an error signal corresponding to a frequency difference between the reference signal and the divided output signal.

43. The wireless transceiver of claim 42, wherein the phase locked loop further includes a charge pump operable to convert the error signal into a charge pump output signal.

44. The wireless transceiver of claim 43, wherein the phase locked loop further includes a loop filter operable to smooth the charge pump output signal and generate a voltage controlled oscillator control signal to control the voltage controlled oscillator.

45. The wireless transceiver of claim 34, wherein the wireless transceiver is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, and 802.14.

46. The wireless transceiver of claim 34, wherein the wireless transceiver is formed as part of an integrated circuit.

47. A wireless transceiver comprising:

means for transmitting a modulated carrier signal, the means for transmitting the modulated carrier signal including means for controlling a frequency of the modulated carrier signal, the means for controlling the frequency of the modulated carrier signal including,

means for generating an output carrier signal having a controlled frequency;

means for generating a dither control signal; and

means for receiving one or more phase signals, each of the phase signals being delayed with respect to the output carrier signal, and generating an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal.

48. The wireless transceiver of claim 47, wherein the interpolated output signal is a weighted sum of one or more of

the one or more phase signals.

49. The wireless transceiver of claim 48, wherein the means for controlling the frequency of the modulated carrier signal further includes means for dividing the interpolated output signal based in part on the dither control signal and generating a divided output signal.

50. The wireless transceiver of claim 49, wherein the means for dividing is operable to fractionally divide the interpolated output signal.

51. The wireless transceiver of claim 49, wherein the means for dividing is operable to divide the interpolated output signal by integers.

52. The wireless transceiver of claim 49, wherein the means for generating an output carrier signal is operable to generate one or more delay signals, each of the one or more delay signals being delayed by a predetermined time period with respect to the output carrier.

53. The wireless transceiver of claim 52, wherein one or more of the one or more input phases are derived based at least in part from the one or more delay signals.

54. The wireless transceiver of claim 49, wherein the means for controlling the frequency of the modulated carrier signal further includes means for generating one or more of the one or more phase signals.

55. The wireless transceiver of claim 49, wherein the means for controlling the frequency of the modulated carrier signal further includes means for comparing a reference signal to the divided output signal and generating an error signal corresponding to a frequency difference between the reference signal and the divided output signal.

56. The wireless transceiver of claim 55, wherein the means for controlling the frequency of the modulated carrier signal further includes pumping means for converting the error signal into a charge pump output signal.

57. The wireless transceiver of claim 56, wherein the means for controlling the frequency of the modulated carrier signal

further includes means for smoothing the charge pump output signal and generating a voltage controlled oscillator control signal to control the voltage controlled oscillator.

58. The wireless transceiver of claim 47, wherein the wireless transceiver is compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, and 802.14.

59. The wireless transceiver of claim 47, wherein the wireless transceiver is formed as part of an integrated circuit.